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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,882	02/27/2004	Paul A. Farrar	303.673US3	9145

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,882	FARRAR, PAUL A.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-22,29 and 36-65* is/are allowed.

6)☒ Claim(s) *1-13,23-28,30-35 and 66-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0506*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 05/03/2006.

Claims 1-79 are active in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 05/03/2006. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

Claim Objection

3. The claim is objected to for the following reason: in claim 23, line 5, the comma "," right before the word "comprising" should be deleted to make the claim be in better format. Appropriate correction is required.

Withdrawal of Allowability

4. The indicated allowabilities of claims 1-13, 23-28, 30-35, and 66-79 are withdrawn in view of the newly discovered reference(s) to Havemann et al. (US 6,358,849), and/or to Edelstein et al. (6,181,012). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim(s) 1, 8, 23, and 30-35 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,181,012 to Edelstein et al.

Regarding claim 1, Edelstein discloses an integrated circuit, as shown in fig. 2, comprising:

a substrate 52 including one or more devices 66;

a first insulating layer overlying the substrate 52 having one or more first level vias (in which plug 62 being formed) connecting to the one or more devices in the substrate 52; and

a second insulating layer 100 (col. 9, lines 50-65) overlying the first insulating layer, the second

insulating layer 100 including one or more conductive structures 46, 78, 72 formed above and connecting to the one or more first level vias, each of the one or more conductive structures including:

a first level metal line 46;

a barrier/adhesion layer 72 having a thickness in the range of 5 to 150 Angstroms (col. 9, lines 27-31, and lines 48-65) formed on the number of first level vias; and

a seed layer 78 having a thickness in the range of 5 to 150 Angstroms (col. 9, line 66 to col. 10, line 13) formed at least between a portion of the barrier/adhesion layer 72 and the first level metal line 46.

Regarding claim 8, Edelstein discloses an integrated circuit, as shown in fig. 2, comprising:

a substrate 52 including one or more devices 66;

an insulator layer overlying the substrate 52, the insulator layer having one or more first level vias (in which plug 62 being formed) connecting to the one or more devices in the substrate 52; and

a polymer layer 100 (col. 9, lines 50-65) overlying the insulator layer, the polymer layer 100 including one or more conductive structures 46, 78, 72 formed above and

connecting to the one or more first level vias, each of the one or more conductive structures including:

a first level metal line 46;

a barrier/adhesion layer 72 having a thickness in the range of 5 to 150 Angstroms (col. 9, lines 27-31, and lines 48-65) formed on the number of first level vias; and

a seed layer 78 having a thickness in the range of 5 to 150 Angstroms (col. 9, line 66 to col. 10, line 13) formed at least between a portion of the barrier/adhesion layer 72 and the first level metal line 46.

Regarding claim 23, Edelstein discloses an integrated circuit, as shown in fig. 2, comprising:

a number of first level vias (in which plug 62 being formed) in a first insulator layer (cover substrate 52) connecting to a number of silicon devices 66 in a substrate 52;

a first number of conductive structures 46, 78, 72 formed over and connecting to the number of first level vias in the first insulator layer, each conductive structure comprising:

a first barrier/adhesion layer 72 having a thickness in the range of 5 to 150 Angstroms (col. 9, lines 27-31, and lines 48-65) disposed on a first level via of the number of first level vias;

a first seed layer 78 formed on at least a portion of the barrier/adhesion

layer having a thickness in the range of 5 to 150 Angstroms (col. 9, line 66 to col. 10, line 13); and

a first core conductor 46 formed on the first seed layer 78;

a polymer 100 (col. 9, lines 50-65) surrounding the first number of conductive structures; and

a second number of conductive structures 56, 60, 76, 72 include a number of second level vias (in which plug 60 being formed) and a number of second level metal lines, wherein the second number of conductive structures are formed over and connect to the first number of conductive structures, and wherein each of the second number of conductive structures includes:

a second barrier/adhesion layer 72 having a thickness in the range of 5 to 150 Angstroms;

a second seed layer 76 formed on at least a portion of the arrier/adhesion layer 72 having a thickness in the range of 5 to 150 Angstroms; and

a second core conductor 56 formed on the second seed layer 76.

Regarding claim 30, Edelstein discloses an integrated circuit, as shown in fig. 2, comprising:

a number of first level vias (in which plug 62 being formed) in a first insulator layer connecting to a number of transistors 66 in a substrate 52 (col. 9, lines 48-65); and

an oxide layer 100 formed over the number of first level vias in the first insulator

layer, wherein the oxide layer 100 includes a number of conductive structures 46, 78, 72 connecting from a top surface of the oxide layer 100 to the number of first level vias, each conductive structure comprising:

a layer of tantalum nitride 72 having a thickness of approximately 5 to 100 Angstroms (col. 9, lines 27-31, and lines 48-65) disposed on a first level via of the number of first level vias;

a seed layer 78 of copper on the layer of tantalum nitride having a thickness of approximately 100 Angstroms (col. 9, line 66 to col. 10, line 13); and

a copper metal line 46 (col. 6, line 62-64; col. 10, lines 3-6) formed on the seed layer of copper.

Regarding claim 31, Edelstein discloses the integrated circuit wherein each conductive structure further includes a layer of tantalum nitride forming a top surface of each 101 conductive structure such that the top surface of each conductive structure is level with the top surface of the oxide layer. See fig. 2.

Regarding claim 32, Edelstein discloses the integrated circuit wherein the oxide layer includes a fluorinated silicon oxide layer. See col. 9, lines 50-65.

Regarding claim 33, Edelstein discloses the integrated circuit wherein at least one of the number of first level vias is filled with tungsten. See col. 6, lines 57-61.

Regarding claim 34, Edelstein disclose the integrated circuit wherein at least one of the number of first level vias is within a titanium silicide liner 72. See fig. 3 and col. 9, lines 28-31.

Regarding claim 35, Edelstein discloses the integrated circuit wherein the integrated circuit is a memory device. See col. 1, lines 17-40; col. 6, lines 60-61.

7. Claim(s) 1-3, 5-9, 11-13, and 23-28 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,538,849 to Havemann et al.

Regarding claim 1, Havemann discloses an integrated circuit, as shown in figs. 1a-l, comprising:

a substrate 102 including one or more devices (transistor having source/drain regions 114);

a first insulating layer 120 overlying the substrate 102 having one or more first level vias (where plug 124 being formed) connecting to the one or more devices in the substrate 102; and

a second insulating layer 122 overlying the first insulating layer 120, the second insulating layer 122 including one or more conductive structures 150, 152, 160 formed above and connecting to the one or more first level vias, each of the one or more conductive structures including:

a first level metal line 160;

a barrier/adhesion layer 150 having a thickness in the range of 5 to 150 Angstroms (col. 3, lines 31-37) formed on the number of first level vias; and

a seed layer 152 having a thickness in the range of 5 to 150 Angstroms (col. 3, lines 38-40) formed at least between a portion of the barrier/adhesion layer 150 and the first level metal line 160.

Regarding claims 2, 3, Havemann discloses the integrated circuit wherein the second insulating layer includes a foamed polymer or foamed polyimide layer. See col. 1, lines 16-33; col. 4, line 49 to col. 5, line 22.

Regarding claim 5, Havemann discloses the integrated circuit wherein the barrier/adhesion layer 150 includes one or more of titanium, zirconium, and hafnium. See col. 3, lines 31-35.

Regarding claim 6, Havemann discloses the integrated circuit wherein the seed layer includes copper and the first level metal line includes a copper metal line. See col. 3, lines 31-49.

Regarding claim 7, Haemann discloses the integrated circuit wherein the integrated circuit is a memory device. See col. 2, lines 20-26.

Regarding claim 8, Havemann discloses an integrated circuit, as shown in figs. 1a-l, comprising:

a substrate 102 including one or more devices (transistor having source drain regions 114);

an insulator layer 120 overlying the substrate, the insulator layer having one or more first level vias (where plug 124 being formed) connecting to the one or more devices in the substrate 102; and

a polymer layer 122 (col. 1, lines 16-33; col. 4, line 49 to col. 5, line 22) overlying the insulator layer 120, the polymer layer 122 including one or more conductive structures 150, 152, 160 formed above and connecting to the one or more first level vias, each of the one or more conductive structures including:

a first level metal line 160;

a barrier/adhesion layer 152 having a thickness in the range of 5 to 150 Angstroms (col. 3, lines 31-37) formed on the number of first level vias; and

a seed layer 150 having a thickness in the range of 5 to 150 Angstroms (col. 3, lines 38-40) formed at least between a portion of the barrier/adhesion layer and the first level metal line.

Regarding claims 9, 11-13, Havemann discloses the integrated circuit comprising all claimed limitations. See the rejections of claims 2, 3, 5-7.

Regarding claim 23, Havemann discloses an integrated circuit, as shown in figs. 1a-l, comprising:

a number of first level vias (where plug 124 being formed) in a first insulator layer 120 connecting to a number of silicon devices (transistor having source/drain regions 144) in a substrate 102;

a first number of conductive structures 150, 152, 160 formed over and connecting to the number of first level vias in the first insulator layer 120, each conductive structure comprising:

a first barrier/adhesion layer 150 having a thickness in the range of 5 to 150 Angstroms (col. 3, lines 31-37) disposed on a first level via of the number of first level vias;

a first seed layer 152 formed on at least a portion of the barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms (col. 3, lines 38-40); and

a first core conductor 160 formed on the first seed layer 152;

a polymer 122 (col. 1, lines 16-33; col. 4, line 49 to col. 5, line 22) surrounding the first number of conductive structures; and

a second number of conductive structures (figs. 1k, l) include a number of second level vias (formed in dielectric layer 170) and a number of second level metal lines, wherein the second number of conductive structures are formed over and connect to the first number of conductive structures, and wherein each of the second number of conductive structures includes:

a second barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms (col. 4, lines 18-40);

a second seed layer formed on at least a portion of the barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms; and

a second core conductor 182 formed on the second seed layer.

Regarding claim 24, Havemann discloses the integrated circuit wherein the second number of conductors is surrounded by a polyimide layer 170&172. See figs. 1k-l.

Regarding claim 25, Havemann discloses the integrated circuit wherein the polyimide layer includes a foamed polyimide layer. See col. 1, lines 16-33; col. 4, line 49 to col. 5, line 22.

Regarding claims 26-28, Havemann discloses the integrated circuit comprising all claimed limitations. See col. 1, lines 16-33; col. 3, line 1 to col. 5, line 22.

Claim Rejections - 35 U.S.C. § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to

a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim(s) 4, 10, and 66-79 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,358,849 to Havemann et al.

Regarding claims 4, 10 Havemann discloses the integrated circuit comprising all claimed limitations, except for wherein first insulating layer includes a Si_3N_4 layer having a thickness between about 100 Angstroms to about 500 Angstroms.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select any suitable dielectric material for the first dielectric layer 120 of Havemann, since selecting a known material on the basis of its suitability for the intended use is just within the general skill of a worker in the art. In re Leshin, 125 USPQ. In addition, a Si_3N_4 dielectric layer would also provide a more selective etchstop for the trench etch. See col. 3, lines 27-30.

Also, it would have been obvious that the dielectric layer may be modified to have a thickness of between about 100-500 Å, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). See further col. 5, lines 23-29.

Regarding claims 66-79, Havemann discloses a system, as shown in figs. 1a-l, comprising all claimed limitations (see the rejections of claims 1-13), except for a processor wherein the integrated circuit being coupled to the processor.

However, it would have been well known in the art at the time the invention was made that an integrated circuit, particularly a memory, could and should be connected or coupled to a processor in order to control the operation of the integrated circuit (or memory device).

Allowance

10. Claims 14-22, 29, and 36-65 have been allowed. See previous communications for reason for allowance.

Conclusion

11. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571)272-1907. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

Dao H. Nguyen
Art Unit 2818
August 25, 2006

DOUGLAS W. OWENS
PRIMARY EXAMINER